A STUDY OF ARCHITECTURE OF FPGA ROUTING

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ABSTRACT

An FPGA is a device that consists of a matrix of reconfigurable gate array logic circuitry. A single FPGA can replace thousands of discrete components by incorporating millions of logic gates in a single integrated circuit (IC) chip. The internal resources of an FPGA chip consist of a matrix of configurable logic blocks (CLBs) surrounded by a periphery of I/O blocks. Signals are routed within the FPGA matrix by programmable interconnect switches and wire routes. The programmable routing in an FPGA provides connections among logic blocks and I/O blocks to complete a user-designed circuit. It consists of wires and programmable switches that form the desired connections. To accommodate a wide variety of circuits, the interconnect structure must be flexible enough to support widely varying local and distant routing demands together with the design goals of speed performance and power consumption. This paper presents an overview of FPGA routing architectures. In commercial architectures, the routing consumes most of the chip area, and is responsible for most of the circuit delay. As FPGAs are migrated to more advanced technologies, then the routing fabric becomes even more important. Thus, there has been a great deal of recent interest in developing the efficient FPGA routing architectures.

KEYWORDS: FPGA, I/O Blocks, IC, Logic Blocks, Routing